Attorney Docket No.: UMC99-001D2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: *Hsuan*	)	Art Unit:
	)	
Serial No.:	)	
	)	Examiner:
Filed: August 5, 2003 as a divisional of serial no. 10/167,118 filed June 11, 2002	)	
	)	
For: *Intermediate Structure for Making Integrated Circuit Device & Wafer*	)	

PRELIMINARY AMENDMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant respectfully submits the following preliminary amendment to place this case in condition for allowance:

AMENDMENTS TO THE SPECIFICATION

Please change the title to read:

-- Intermediate Structure for Making Integrated Circuit Device & Wafer --

Please add the following text at page 1, line 5:

-- CROSS REFERENCE TO RELATED APPLICATIONS

The present application is a divisional of serial no. 10/167,118 filed June 11, 2002 entitled *Integrated Circuit with Improved Interconnect Structure and Process for Making Same*, which application in turn is a continuation of serial no. 09/304,244, now U.S. Patent No. 6,429,509, both of which are hereby incorporated by reference. --

Please substitute the following for the text at page 2, ll. 24 – 30:

A typical flip chip type package 100 known in the art is depicted in FIG. 1. It can be seen here that chip package 100 includes a number of bonding pads 110, which are located in a pad area 115 surrounding die (chip) area 120. A total area 130 for package 100 ~~110~~ can be seen to be comprised of two distinct sub-areas, therefore, including bonding pad area 115, and die area 120. Again, for a whole number of reasons, including throughput, productivity, cost, and performance considerations, the size of bonding pads 110, and thus area 115, should be kept small compared to the area of chip area 120.

Please substitute the following for the text at page 7, ll. 23 – 30:

By avoiding the need for I/O pads on the top of die 230 ~~200~~, a wafer manufactured in this way will have increased circuit density, reliability, yield and throughput. Of course, nodes 210 can also be made to be as large as conventional I/O bonding pads, and in some environments it may be desirable to have some portion of the I/O signals accessible in this manner to other interconnects coupled to the top surface of die 230. In general, however, one of the primary goals and benefits of the present invention is the ability to reduce the amount of usable die circuit wafer processing area needed to establish I/O interconnects (including power and ground) to external circuits. Accordingly, a preferred embodiment of the present invention ~~implements~~ minimizes the die top surface area taken

Please substitute the following for the text at page 15, ll. 1 – 26:

reference. Generally speaking, however, in the present embodiment, solder bumps 550 are preferably formed from a material that has a low contact resistance, because it is intended to be used with a mating receptacle 560 as shown in FIG. 5C. Accordingly, since this material is not intended to be reflowed, or soldered, it can be formed of any convenient substance, including, for example gold, nickel, or even Tin, Tin/lead and other low cost alloys. As shown in FIG. 5C, this mating receptacle 560 includes a recessed area large enough to receive the body of die 500 in a frictional contact fit. This frictional fit arises as a result of solder bumps 550 ~~500~~ contacting opposing mating surface 551, the latter which is preferably a low resistance contact pad made of a substance such as gold, or particle enhanced interconnect material. As seen in FIG. 5D, these mating pads then carry the various I/O signals from circuit area 520 through pins 563 to other circuits which may be located, for example, on a printed circuit board. It is apparent, of course, that the arrangement of solder bumps 550 and mating surface 551 can be reversed - i.e., that die 500 can use pads, and that mating surface 551 can be formed as a bump - to achieve the same result. The benefit of the present arrangement can be seen in the fact that this form of interconnect is extremely easy to assemble (and thus cost effective) because it can be accomplished by simply applying a small amount of mechanical force applied to the die 500 so that it snaps into place within mating receptacle 560. In this way, conventional soldering, reflow, or adhesive type mating arrangements of the type shown in U.S. Patent No. 5,682,062 are eliminated, but yet the advantages of a highly integrated die (i.e., with no wasted active area for contact pads) can be preserved. The solder bumps and mating contacts can be made of relatively inexpensive materials as well, since they only need to form a single contact (usually) during the lifetime of the device. In other words, it is expected that the die itself may have to replaced at most a couple of times, so there is no need to make the contact surfaces extremely durable, as would be the case for a part that would require many insertions and removals.